Claim 1. (Original) A method of fabricating complementary metal oxide semiconductor (CMOS) devices on a semiconductor substrate, featuring a silicon - germanium (SiGe), layer used as a component of a CMOS device channel region, with the integration of a selective epitaxially deposited, strained SiGe channel layer in a CMOS process performed after formation of isolation regions, comprising the steps of:

providing a first region of said semiconductor substrate to be used as an NMOS (N channel metal oxide semiconductor) region, and providing a second region of said semiconductor substrate to be used as a PMOS ( P channel metal oxide semiconductor) region;

forming isolation regions in top portions of said semiconductor substrate;

forming a P well region in said NMOS region, and forming an N well region in said PMOS region;

selectively depositing a composite silicon layer on the top surface of portions of said semiconductor substrate not occupied by said isolation regions, with said composite silicon layer comprised of said SiGe layer, and comprised of an overlying silicon layer; and

forming a gate insulator layer on said overlying silicon layer.

Claims 2 - 27 (cancelled)

Claim 28 (new) A metal oxide semiconductor field effect transistor (MOSFET) structure on a semiconductor substrate, comprising;

insulator filled shallow trench shapes comprised of underlying bottom portions featuring straight sides and extending from a level equal to the top surface of said semiconductor substrate downwards into a top portion of said semiconductor substrate, and with said insulator filled shallow trench shapes comprised with overlying top portions featuring tapered sides, and wherein said overlying top portions of said insulator filled shallow trench shapes extend upwards to a level between about 1000 to 2000 Angstroms above the level of the top surface of said semiconductor substrate;

a composite semiconductor shape on a top surface of said semiconductor substrate, with said composite semiconductor shape featuring tapered sides, and located between said overlying top portions of said insulator filled shallow trench shapes;

insulator filled V groove shapes located between said composite semiconductor shape and said overlying top portions of said insulator filled shallow trench shapes;

a conductive gate structure on an underlying gate insulator, located on a portion of said top surface of said composite semiconductor shape;

insulator spacers on sides of said conductive gate structure; and

a source/drain region in a portion of said composite semiconductor substrate not covered by said conductive gate structure or by said insulator spacers, with said source/drain region extending into an underlying portion of said semiconductor substrate.

Claim 29 (new) The MOSFET structure of claim 28, wherein said insulator filled shallow trench shapes are comprised of silicon oxide, with said underlying bottom portions of said insulator filled shallow trench shapes extending to a depth between about 3000 to 6000 Angstroms in said semiconductor substrate.

Claim 30. (new) The MOSFET structure of claim 28, wherein said composite semiconductor shape is comprised with an underlying silicon shape at a thickness between about 0 to 100 Angstroms, a middle shape at a thickness between about 20 to 150 Angstroms comprised of strained silicon - germanium (SiGe), and an overlying silicon shape at a thickness between about 20 to 150 Angstroms.

Claim 31. (new) The MOSFET structure of claim 28, wherein a middle shape of said composite semiconductor shape is comprised of strained SiGe with a germanium content between about 20 to 40 weight percent.

Claim 32. (new) The MOSFET structure of claim 28, wherein said insulator filled V groove shapes are comprised of silicon oxide.